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ADVANCED MICRO DEVICES, INC.
C/O VEDDER PRICE P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
HSU, JONI	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

As per Claim 29, Examiner agrees that combination of references do not teach alternate frame rendering by rendering entire temporally adjacent frame of video, provided same output port, as argued by Applicant (pages 8-9). The rejection of Claim 29 is withdrawn.

As per Claim 30, Applicant argues Walls (US006215496B1) teaches each computer generates partial frame of entire logical scene. None of computers generates entire frame of video that are output over common port. Walls requires plurality of independent ports (p. 7-8).

In reply, Examiner points out even though Walls teaches each computer generates portion of "logical frame", this portion of "logical frame" is considered to be entire frame of video, since each computer generates video for entire screen for one display device (c. 2, ll. 39-41). Lengyel (US006016150A) was used to teach common port.

Applicant argues both Walls and Lengyel teach composite processing of single frame as opposed to alternating frame rendering scheme (p. 8).

In reply, Examiner points out Claim 30 does not specify that frames are alternating.

As per Claim 1, Applicant argues office action alleges frame buffer 430 is second video output port, however frame buffer is not video output port (p. 10).

Examiner understands frame buffer 430 of Normile (US005461679A) is not video output port in and of itself. But, frame buffer 430 outputs to display 440 (c. 10, ll. 3-17). So, even though Normile does not explicitly teach “second video output port”, there must be video output port connected between frame buffer 430 and display 440 in order for data from frame buffer 430 to be output to display 440. So, Normile is considered to teach 2nd video output port.

Applicant argues claim requires first video component output provides first video output component signal. This does not appear to be addressed in office action. Office action on one

hand alleges that video output port is frame buffer 430 and then on the other hand, alleges that video output port is bus. Claim interpretation must be consistent (p. 10-11).

In reply, Examiner points out Normile discloses "dual-port memory 504 is coupled to control bus 412 for communication between computing module 401 and device over bus 425 such as host 410 and display controller 426" (c. 10, ll. 30-32). Since video processing module 401 (c. 9, ll. 11-15) outputs to bus 425 over bus 412, bus 412 is considered to be first video component output. Since bus 412 outputs from video processing module 401, bus 412 outputs first video output component signal. Bus 425 outputs to display controller 426, and connection between bus 425 and display controller 426 is depicted by line with arrows pointing in opposite directions in Fig. 4. So, even though Normile does not explicitly teach "first video output port", since bus 425 outputs to display controller 426, there must be video output port connected between bus 425 and display controller 426, which is depicted by this connecting line. There must be 2nd video output port connected between frame buffer 430 and display 440 as discussed above, and this is depicted by line connecting frame buffer 430 and display 440 in Fig. 4.

Applicant argues bus 425 does not provide data to bus 420 nor does bus 420 provide data on bus 425 (p. 11).

In reply, bus 420 outputs to shared memory 405, which outputs to bus 425 (c. 9, ll. 48-58), and so bus 420 provides data on bus 425, and so bus 420 is coupled to bus 425.

As per Claim 18, Applicant argues interpretation of Normile with respect to Claim 1 is inconsistent with interpretation being taken with respect to Claim 18 which cites Taylor (US006118461A) since alleged video output ports for which Normile is cited as teaching, would

require monitor to be coupled to bus 425 which clearly it is not as shown in Normile. Normile is coupled to frame buffers 427 or 430 (p. 11).

In reply, Normile teaches frame buffers 427, 430 are coupled to monitors 428 and 440, and so bus 425 is still considered to be coupled to monitor 428 (c. 9, ll. 20-24; c. 10, ll. 3-17).

As per Claim 19, Applicant argues adjustment is with respect to color component values, not timing or synchronization signals as taught in Deering (US005963200A) (p. 12).

In reply, Examiner points out Gonsalves (US006847373B1) was used to teach this.